In the Specification:

The abstract is amended as folllows:

~~The present invention provides a method and~~ An apparatus that improves Built-In-Self-Test (BIST) flexibility ~~without requiring the complexity of a compilable BIST circuit~~. ~~Additionally, the present invention provides the ability to use a single BIST to test multiple memory arrays of different sizes. The preferred embodiment of the present invention provides a~~ A compilable address magnitude comparator ~~to~~ facilitates BIST testing of different size memory arrays without requiring customization of the BIST controller. The ~~preferred embodiment~~ compilable address magnitude comparator is compiled within the compilable memory arrays of the ASIC to allow a single BIST controller to test multiple sizes of memory arrays without requiring that the BIST controller ~~itself~~ be compilable. ~~In the preferred embodiment, the~~ The compilable magnitude address comparator overrides the self-test signal from the BIST when the BIST attempts to test addresses ~~that do~~ not existing in memory. ~~As such, the~~ The BIST is prevented from writing to addresses that do not exist, and does not receive error signals from those addresses. ~~Thus, the~~ The BIST controller is able to test memory arrays without regard for their particular size. A single BIST controller can ~~then~~ be used to test multiple memory arrays of different sizes in the ASIC, ~~again~~ reducing device complexity.